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Nuts and Bolts of Core and **SoC Verification** - all 14 versions »
K Albin - 38th Design Automation Conference (DAC'01), 2001 - doi.ieeecomputersociety.org
... 3.1.3 the ability to organize large amounts of data **SoC** designs are large ... Monitors Figure 1 shows the basic components of a unit-level **verification testbench**. ...
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[BOOK] Surviving the **Soc** Revolution: A Guide to Platform-Based Design
H Chang - 1999 - Kluwer Academic Publishers
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[BOOK] System-On-A-Chip **Verification**: Methodology and Techniques - all 2 versions »
P Rashinkar, P Paterson, L Singh - 2001 - books.google.com
... This anecdote motivates this book on **SOC verification**. Effec -tive **verification** is fundamental to design reuse ... be accompanied by a reusable "complete" **testbench** ...
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Verification of configurable processor cores - all 10 versions »
M Puig-Medina, G Ezer, P Konas - Annual ACM IEEE Design Automation Conference: Proceedings of ..., 2000 - doi.ieeecomputersociety.org
... **TESTBENCH** Emulated System Monitors ... the processor RTL, the **verification** suite, and the system **test-bench**. ... be easily merged into an **SOC verification** environment. ...
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[PDF] Practical Approaches to **SOC Verification** - all 2 versions »
G Mosensoson - Proceedings of DATE User Forum, 2000 - cecs.uci.edu
... effect they have on the design of the **testbench**. The rest of this paper focuses on showing practical and novel approaches to the **verification** of **SOC** designs. ...
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C-based **SoC** design flow and EDA tools: an ASIC and system vendorperspective
K Wakabayashi, T Okamoto - Computer-Aided Design of Integrated Circuits and Systems, ..., 2000 - ieeexplore.ieee.org
... and semi-formal verifiers, and **test-bench** generators. The **verification** tools are tightly integrated with the HLS ... feature into the C-based **SoC** design environment ...
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A framework for object oriented hardware specification, **verification**, and synthesis - all 18 versions »
T Kuhn, T Oppold, M Winterholer, W Rosenstiel, M ... - Proceedings of the Design Automation Conference (DAC'2001), 2001 - doi.ieeecomputersociety.org
... **Testbench** in 'e' eSS ... environment may be subject to synthesis which may facilitate **test bench** acceleration and ... Practical Approaches to **SOC Verification**. ...
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R Devins - IEEE/DATC Electronic Design Processes Workshop, April, 2001 - eda-stds.org
... System **verification** often involves external, or off-chip data ... consider the off-chip